

## An Improved Single Phase Full Bridge Inverter Using Sequential Triggering for Achieving Zero Voltage without Inductor

استخدام الاشعال المتتابع لتحسين عاكس قنطرة كاملة احادي الوجه للحصول على جهد صفر بدون استخدام ملف

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يقدم هذا البحث طريقة جديدة لاشعال دوائر العاكس المستخدمه في التحكم في سرعه لمحركات او في الاكترونيات الصناعيه. و تستخدم هذه الطريقه دوائر الاشعال التتابعي الزماني. هذه الدوائر مصممه بحيث تعطى نبضات لاشعال مفاتيح العاكس و كذلك تعطى زمن تاخير بين هذه النبضات. هذا الزمن لازم لكي لا يحدث تدخل بين نبضات الفرع الاول و الفرع الثاني في عاكس القنطره الكامله. مما يضمن تشغيل اشل دوائر العاكس و نتيج هذه الطريقه انتقال التيار بين فرعي العاكس بدون حدوث قصر بين فرعي العاكس. و قد تم اختبار لداء العاكس مع البطاريات و كذلك الخلايا الشمسيه و قد تبين ان العاكس يعمل بكفاءه عاليه و كذلك تم تصميم المنظومه بالكامل.

### **Abstract:**

This paper introduces new technique for triggering full bridge inverter based on power transistor as switches. This method based on the design of a sequential timer as triggering circuits. The designed timer is designed to trigger the power switches of the two branches of the inverter and provides enough delay time between the triggering signals of the inverter branches. The interval of the delay time must be properly chosen to ensure that the current of branch reaches to its zero before applying the triggering to the second branch of the inverter. Consequently, the load current crosses the zero value and goes down safely to the negative direction. In this paper the full bridge inverter based on power transistor, control strategy for triggering, interface stages between the timer and the transistors bases are designed. The system undergoes is tested by using the lead acid battery and the solar cells array as a power supply. The system offers efficient operation with the two supplies.

### **Introduction**

Single phase full bridge inverter (SPFBI) is used in wide range for transferring the DC-to AC. It used also for motor drive. The main problem for the inverter is how to trigger the inverter taking into account the time duration which the power switches still on after removing the triggering signal. This time is equal to the power transistor storage time plus its falling time. This problem is very important

since the power switch is still on. So the transistors of each branch of the bridge inverter would be still on after removing the triggering signal by a time equal to the transistor off time [1]. This phenomenon is not desired during the operation. Most triggering circuit such as astable multivibrator circuits provides pulses with no phase shift or time delay. This problem requires an application of soft-switching circuit [2], or using a zero-voltage power switch, which may increase the electromagnetic interference [EMI] and requires a complicated snubber

circuit [3]. Therefore the cost of the inverter is increased. The efficiency of it may be reduced also and in some cases requires a large LC-filter circuit.

### Analysis of Operation

The full bridge of a single phase inverter, which uses four switching devices (power transistor, GTO, IGBT,tc), is the most common type of inverters. Since the source voltage is switched at regular intervals to produce an alternating output voltage. Varying the pulse width of each cycle of the triggering pulse controls the output of the inverter. This technique is accomplished by changing the control strategy of the transistor triggering. Figure 1 shows a single phase inverter using the power transistors as switches.

When switches Q1 and Q3 are on the current flow from left to right, and when switches Q2 and Q4 are turned on (in the same time Q1 and Q3 are off), the current flows from right to left producing the negative half cycle of the waveform. Hence, an alternating current is produced. The pulse sequence on the bases of the power switches and the inverter output voltage are illustrated in table 1. When the pulse signal is applied to the base of Q1 and Q3, the output voltage will be equal to +E (where E is the DC voltage level to be converted). On the other hand, the application of the triggering pulse on Q2 and Q4 bases results in an output voltage level of -E. The results are a variable voltage output alternates between +E and -E

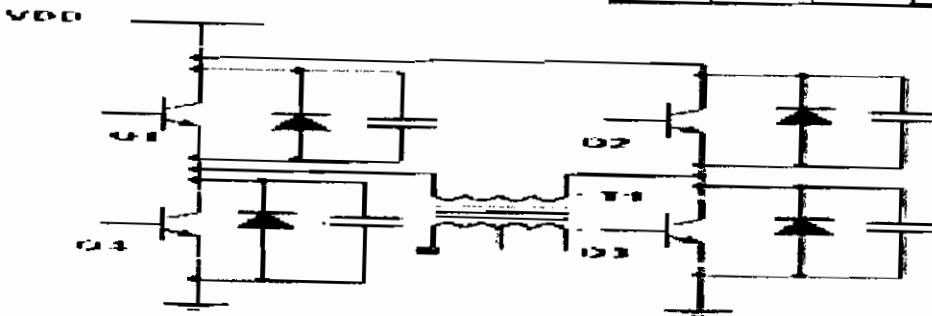


Figure 1. the single phase inverter bridge based on the power transistor switches

levels. The main problem is that when the triggering pulse is provided to Q2 and Q4 bases at the falling edge of Q1 and Q3 pulses, Q1 and Q3 transistors are still on ( since the transistor is on during its off time ). Consequently, the pulse applied to Q1 and Q3 must be terminated earlier before applying the pulses to Q2 and Q4 bases. Otherwise, the failure due to secondary breakdown is carried out [4].

By proper designing of a proposed trigger circuit involves sequential timer (ST), time delay circuit and interface stages between the inverter switches and the sequential timer based on proposed control strategy. Proper design of the sequential timer circuit results in a time delay between the applicable pulses on the inverter power switches. Figure 2 shows the topological circuit of the designed sequential timer. It has four stages consists of an astable multivibrator and three cascaded monostable multivibrator circuits. The proposed trigger circuit is designed for producing two pulses with a selected time delay between them. This time must be equal or slightly greater than the power switch off time. The frequency of each pulse is the same and equals to the inverter output.

Table 1 the power switch status and the corresponding output voltage.

| Q1  | Q2  | Q3  | Q4  | Vo |
|-----|-----|-----|-----|----|
| on  | off | on  | off | +E |
| off | on  | Off | on  | -E |

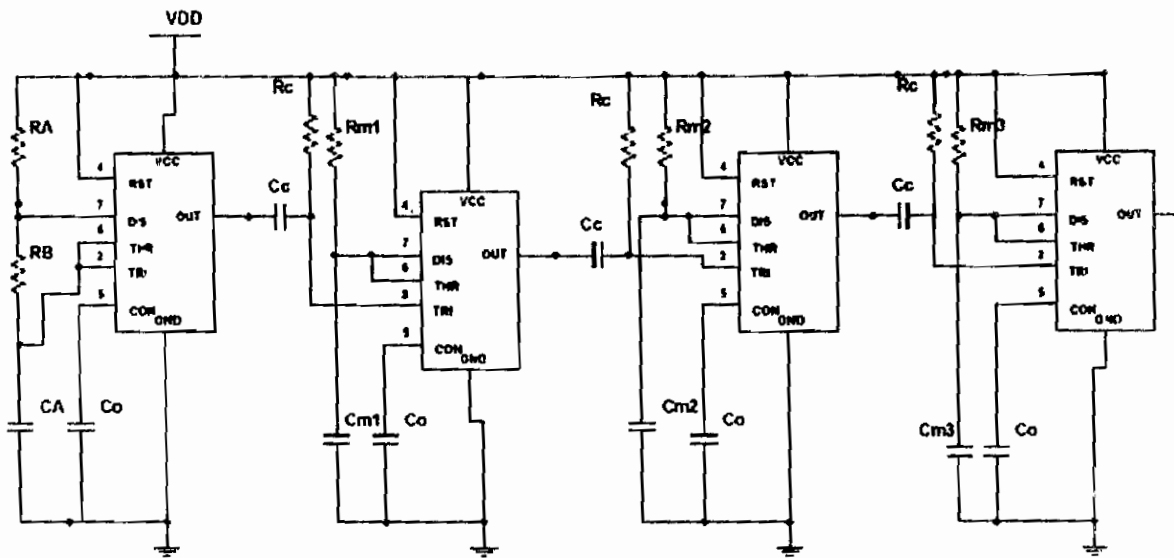


Figure 2. The sequential timer for producing the pulses with a time delay

### Design of Triggering Circuit

The main circuit designed for triggering the inverter power switches is composed of two main parts. The first part of the circuit is a sequential timer circuits. The second part is the interface stages connecting between low rate trigger circuits (sequential timer, ST) and the high rate power switches. An accurate design of each part is introduced in this paper.

#### Design of Sequential Timer Circuits

The sequential timer under design contains four circuits. The first one is the astable multivibrator (ASM) for obtaining a train of pulses with frequency of 50 Hz. The second stage of the timer is designed as a monostable multivibrator (MONO1) which produces a pulse with 9.99995 ms pulse width for driving power switches Q1 and Q3 simultaneously. The third stage of the timer, MONO2, is designed for producing a pulse with pulse width slightly greater than the transistor off time. The output of MONO2 is triggered the fourth stage of the

timer which is designed as a MONO3. The output of MONO3 generates the pulse required for driving switches the power transistors Q2 and Q4.

#### Design of Astable Multivibrator

The astable multivibrator under design must produce a pulse with frequency of 50 Hz and duty cycle of 98%. Design of the astable multivibrator circuit depends on IC555 time data sheet specifications. The charging current of capacitor  $C_A$ ,  $I_c$ , must be selected such that [5];

$$I_c \gg I_{th}, \text{ and} \quad (1)$$

$$I_c \gg I_{tri}, \quad (2)$$

Where  $I_{th}$  is the IC555 threshold current and  $I_{tri}$  is the IC555 triggering current. The value of  $I_{th}$  and  $I_{tri}$  are obtained from the timer data sheet which are equal to 0.25  $\mu$  and 0.5  $\mu$  respectively. Consequently, the values of  $I_c$  is selected as 1mA.

The design values of  $R_A$ ,  $R_B$  and  $C_A$  are given from the following equations:

$$R_A + R_B = \frac{V_{cc}}{3I_{c(\min)}} \quad (3)$$

$$C_A = \frac{t1}{0.693(R_A + R_B)} \quad (4)$$

$$R_B = \frac{t2}{0.693C1} \quad (5)$$

The typical values of the designed elements are equals to 3198, 81.6 and 7.07  $\Omega$  respectively. Figure 3a represents the shape of output pulse of the astable multivibrator as the circuit simulated by multisim program. On the other hand, Figure 3 b introduces the experimental output pulse from the designed multivibrator circuit recorded by the oscilloscope.

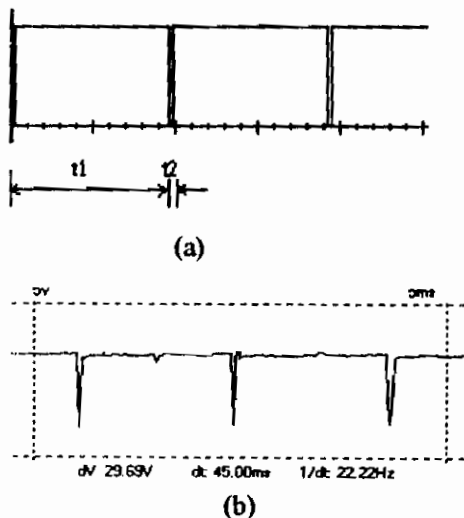


Figure 3. astable output by (a) as simulated by multisim program, (b) by the experimental result.

The typical value of  $R_{m1}$  and  $C_{m1}$  are 160 k $\Omega$  and 56.8 nF respectively. Figure 4. represents the output pulses of the astable (Figure 4a) and MONO1 multivibrator (Figure 4b) as given by the simulation program as well as the experimental pulse output from MONO1 (Figure 4c).

### Design of Monostable Multivibrator

The monostable 1 multivibrator (MONO1) is triggered by the output signal from the previous astable multivibrator. At the trailing edge of the astable multivibrator output initiates the MONO1, the output pulse width (PW1) of MONO1 must be designed such that

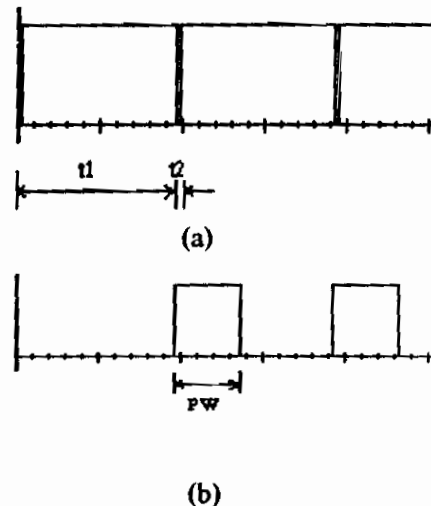
$$PW = \frac{T}{2} - T_{off} \quad (6)$$

Where  $T$  is the periodic time of the inverter output waveform and  $T_{off}$  is the power transistor off time.

The schematic diagram of MONO1 is illustrated in Figure4. The elements of MONO1 circuit are designed from the following equation:

$$R_{m1} = \frac{V_{cc}}{3I_{cc}} \quad (7)$$

$$C_{m1} = \frac{PW}{1.1R_{m1}} \quad (8)$$



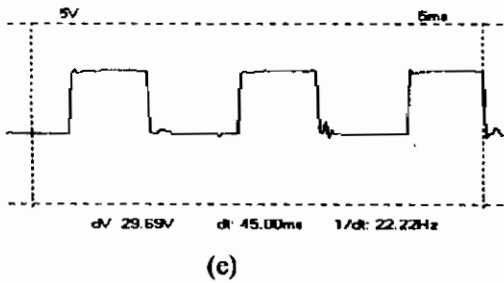


Figure 4. The MONO1 output with the astable as a trigger for MONO1: (a) Astable output, (b) MONO1 output by simulation, (c) experimental results of mono1.

**. Design of Monostable 2 Multivibrator**

The MONO2 is illustrated in Figure 2 as a third stage of the sequential timer. This multivibrator is used for triggering the MONO3 after MONO1 by a time interval equal to the power transistor turn off time. Hence its output pulse must be accurately equal to  $T_{off}$ . For the simplicity of the design procedure  $R_{m2}$  is selected equal to  $R_{m1}$ . The capacitance  $C_{m2}$  is obtained as follows,

$$C_{m2} = \frac{T_{off}}{1.1R_{m2}} \quad (9)$$

It this has a typical value of 2.84 pF. Figure 5 shows the experimental output pulse of MONO2,

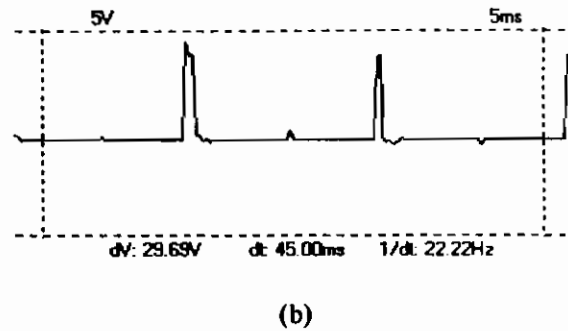
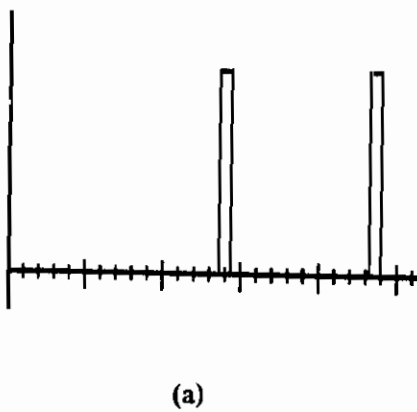
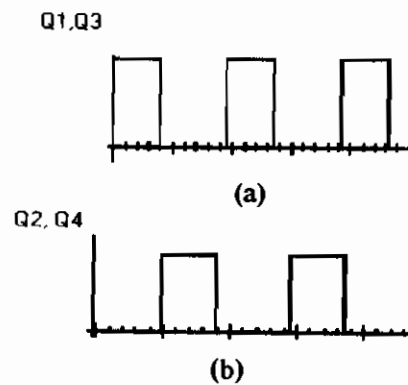


Figure 5. the output of the MONO2: (a) by the simulation program, (b) by the experimental results.

**Design of Last Stage of Sequential Timer**

The last stage sequential timer under design as illustrated in Figure 2 is a MONO3. The MONO3 is designed such that its pulse output has the same specifications of the output pulse of MONO1. This means that, MONO1 and MONO3 output pulses have the same pulse width and frequency. Consequently, the design of MONO3 electrical elements  $R_{m3}$  and  $C_{m3}$  are similar to that of MONO1 and they have the same value of  $R_{m1}$  and  $C_{m1}$ . The output pulse of this multivibrator is used for triggering the power switches  $Q_2$  and  $Q_4$ . Figure 6 represents the output pulse from MONO1 (Figure 6a), which triggers the power switches  $Q_1$  and  $Q_3$ , MONO2 (Figure 6b), which triggers  $Q_2$  and  $Q_4$  along with the inverter output wave form (Figure 6c).





this Figure shows the complete circuit including the trigger sequential circuit, the interface circuit and the inverter bridge circuit.

**Experimental Performance of the Inverter**

Figure 8 measures the output voltage with insolation as an evaluation of the inverter performance feeds directly from solar cell array. This Figure shows the relation between the output load voltage at different levels of insolation over the day light to evaluate the inverter performance with the solar insolation.

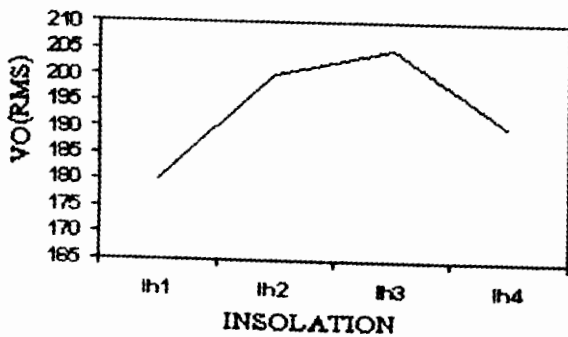


Figure 8. measured output voltage of the experimental inverter with the different level of insolation.

This Figure shows that the output voltage may vary with the variation of the insolation, since the insolation is not constant over the day time and absent at the night.

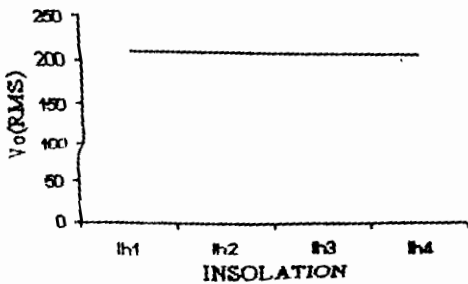
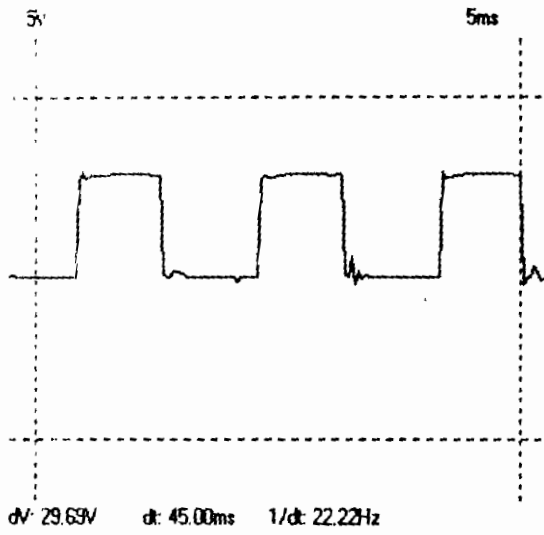


Figure 9. the circuit feed directly from the battery.

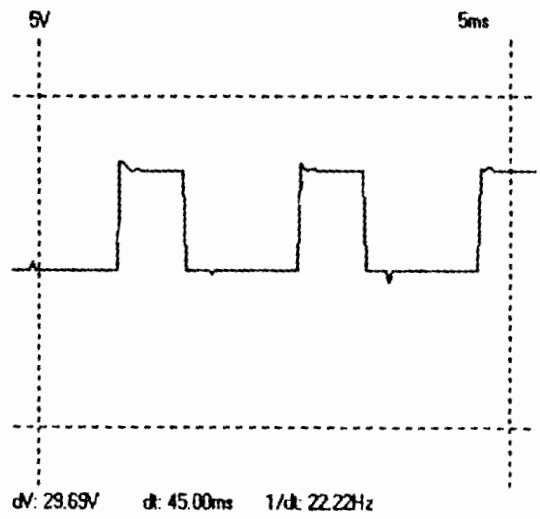
So we must use a battery as a storage system to feed the system with constant voltage and provide continuous operation during the night. The relation between output voltage and time when the inverter is fed from the battery as shown in Figure 9 indicates that the output voltage is more stable and has low variations in its value with the time. So the battery is the essential component in the standalone photovoltaic system to reduce the time-variation of the voltage, this leads to nearly constant voltage during the operation. Another parameter may affects the output voltage is the pulse width of the triggering circuit. Since the control of the output voltage can be achieved by changing the trigger circuit pulse width or by changing the triggering pulse frequency.

**Experimental Results**

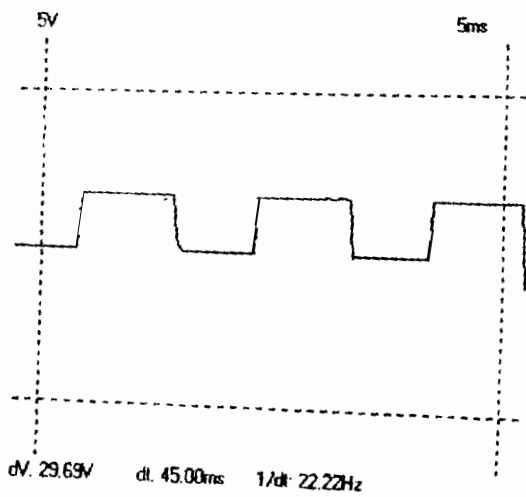
Figure 10 shows the experimental results for the waveform of the sequential circuit and the inverter. These waveforms illustrate turn-on and turn-off switches characteristics of the main device under considering the time-delay in order to verify the zero voltage transition without any continuous operation of the power switch in the inverter bridge. The interface circuit directly coupled with the sequential timer on off characteristics is represented by this figure as an example of the whole stages of the interface circuit.



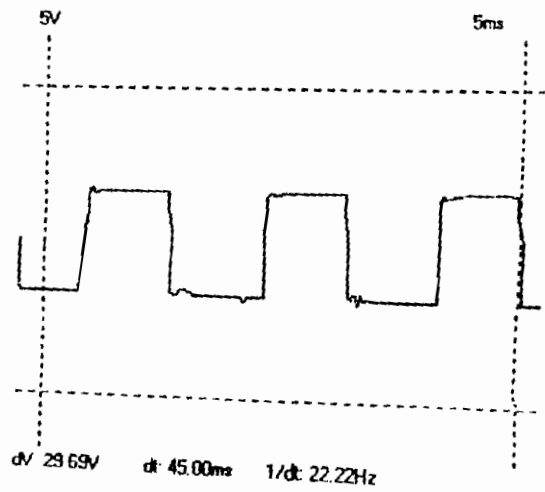
(a) MONO 1 output



(b) MONO 2 output



(c) Interface 1 circuit output



(d) transformer output

Figure 10 experimental output waveforms from different parts of the inverter circuits.



### Conclusions

In this paper, an improved method for the single phase inverter was designed to achieve zero-voltage transition, without complicated snubber circuit or soft-switch circuit. The application of these circuits increases the cost and the complexity of the inverter circuits. A comprehensive analysis of the proposed circuit indicates the zero-voltage transition without using inductor in the circuit. Hence, this method is characterized by the simplicity and low cost. The simulation results were found to be in a good agreement with experimental results indicating that zero-voltage operation during transition was achieved by designing the proposed circuits..

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