Mansoura University Faculty of Engineering Electronics and Communications Engineering Department

Digital Circuits 1 - COM 9124	Exam Time: 3 hours
Exam Date: June 5th, 2013	Total Marks: 70 Marks
1st year Electronics - 2nd Term	Closed Book term exam

Important Instructions:

1 This exam contains 6 questions:

Q1) 10 MCQs (4 choices each) --> Mark your answer selection in the MCQ answer sheet in the middle of the answer booklet Q1-Q15

(page 2 - 15 Marks)

Q2) 10 Questions (Fill the blanks with pre-selected words) --> Write ONLY your answers in the answer booklet

(page 3 - 15 Marks)

Q3-Q6) 4 Regular technical questions --> Write your answers in the answer booklet

(pages 3 & 4 - 40 Marks)

2 Use "MCQ + 4 pages" answer sheet.

3 Atempt all questions.

4 No calculators are allowed in this exam.

5 No external materials are allowed in this exam.

My best wishes to YOU!

Dr. Sameh Rehan

Note: This exam has questions on both sides of the two questions' sheets.

Q1) **Answer the following 10 MCQs in the MCQ sheet in the answer booklet:**
(+1.5 Marks for each correct answer, zero Mark for each wrong answer, zero Mark for unanswered question) **(Total of 15 Marks)**

Q1-1 A circuit that converts a digital waveform to an analog signal is commonly called a(n) _____.
① PLD ③ DAC
② ADC ④ CAD

Q1-2 When using negative logic _____.
① HIGH = 1 and LOW = 0 ③ HIGH = 0 and LOW = 1
② HIGH = 0 and LOW = -1 ④ LOW = -1 and HIGH = 1

Q1-3 The math symbol for time of transition from HIGH to LOW is _____.
① t_r ③ t_w
② T ④ t_f

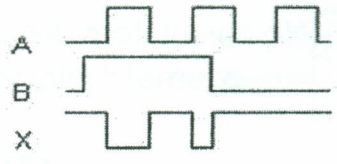
Q1-4 For a negative-logic pulse, the leading edge is the _____.
① LOW-to-HIGH transition ③ rising edge
② positive-going edge ④ negative-going edge

Q1-5 The output of an AND gate is HIGH _____.
① only when all inputs are LOW ③ when at least one input is LOW
② only when all inputs are HIGH ④ no answer is correct

Q1-6 Two kinds of data selectors are _____ and _____.
① encoders, decoders ③ comparators, registers
② multiplexers, demultiplexers ④ adders, subtractors

Q1-7 Which converts data from a serial to a parallel form?
① Comparator ③ Encoder
② Demultiplexer ④ Multiplexer

Q1-8 This is the timing diagram for a 2-input _____ gate.



① NAND
② AND
③ XOR
④ NOR

Q1-9 This is the truth table for a(n) _____.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

① OR
② NOR
③ AND
④ NAND

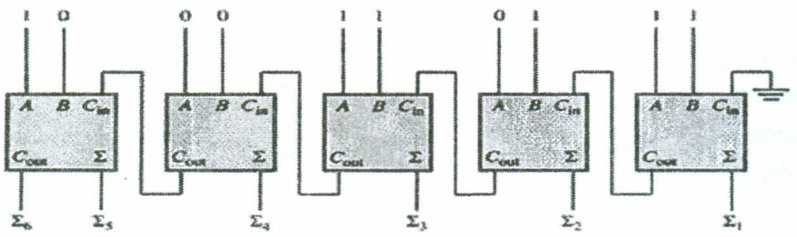
Q1-10 The number of binary digits that are required to count to decimal 60 is:
① 7 bits ③ 6 bits
② 8 bits ④ 5 bits

Closed book term exam	**3 hours - 70 Marks**
Digital Circuits 1 - 2nd term - COM 9124	**June 5th, 2013**
1st year electronics engineering students	**page 4 of 4**

Q5) **(total of 10 marks)**

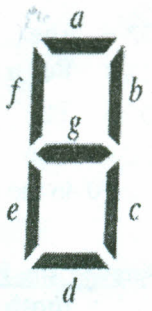
a- Draw the basic logic diagram (using only basic logic gates) of a decimal-to-BCD encoder. **(total of 5 marks)**

b- For the shown parallel adder, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers. **(total of 5 marks)**



Q6) **(total of 10 marks)**

For the 7-segment decoding logic, a BCD number is used as the input and the 7 outputs are used to activate the corresponding segments of the display. The arrangement of segments is as shown here:



a- write down the truth table (use X to represent don't care output) for all 7 segments. **(4 marks)**

b- develop the optimized <u>product of sum</u> Boolean logic expression of the "e" output segment using Karnaugh map. **(3 marks)**

c- develop the optimized logic circuit using only NOR gates. **(3 marks)**

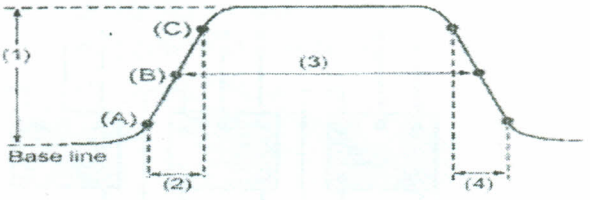
Closed book term exam	**3 hours - 70 Marks**
Digital Circuits 1 - 2nd term - COM 9124	**June 5th, 2013**
1st year electronics engineering students	**page 3 of 4**

Q2) **Fill the blanks (by selecting from the listed words) in the answer booklet for the following questions:**

(+1.5 Marks for each correct answer, zero Mark for each wrong answer, zero Mark for unanswered question) (Total of 15 Marks)

(NOT, OR, AND, NAND, NOR, XOR, XNOR, rise time, fall time, amplitude, transition time, period, pulse width, zero, infinite, positive-going edge, negative-going edge, Multiplexer, Demultiplexer, Encoder, Decoder, LOW, HIGH)

In the shown nonideal pulse:



Q2-1 Item (1) represents _____.
Q2-2 Item (2) represents _____.
Q2-3 Item (3) represents _____.
Q2-4 Item (4) represents _____.

Q2-5 The _____ gate performs as switches wired in parallel.

Q2-6 The _____ gate can be used to add two bits.
Q2-7 For a positive-logic pulse, the trailing edge is the _____.
Q2-8 The _____ circuit creates an output LOW to indicate that the input values are equal.
Q2-9 The _____ circuit converts a specific coded form into known information.
Q2-10 In the NOT digital circuit, a _____ input gives a HIGH output.

Answer the following regular questions in the answer booklet: (4 questions)
(both wrong answers and unanswered questions have zero marks)

(total of 40 marks)

Q3) For the half-subtractor logic circuit: **(total of 10 marks)**
a- draw the logic symbol. **(2 marks)**
b- write down the truth table. **(2 marks)**
c- develop the logic implementation using only basic logic gates. **(3 marks)**
d- form a full-subtractor circuit using half-subtractors and any required gates. **(3 marks)**

Q4) **(total of 10 marks)**

If the data-select inputs to the shown multiplexer are sequenced as shown by the shown waveform determine the output for the following input state
Do = 1, D1 = 0, D2 = 0, D3 = 1